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L17	(packing or pack$1 or packed or compact$3 or compress$5) near5 (data or byte$1 or word$1 or bit$1)	136978	L17
L16	L13 and l6	37	L16
L15	L13 and l5	396	L15
L14	L13 and l4	11	L14
L13	L12 and (less or greater or equal or le or eq or gt or lt) near12 (psw or overflow or zero or carry or sign$1)	3367	L13
L12	L1 near6 (select$6 or mask$6)	7921	L12
L11	l7 and l6	16	L11

L10	l7 and l5	100	L10
L9	l3 and psw	11	L9
L8	l2 and psw	83	L8
L7	l3 and (less or greater or equal or le or eq or gt or lt) near12 (psw or overflow or zero or carry or sign$1)	347	L7

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L3	L2 near15 (mask$6 or reset$5 or updat$6)	558	L3
L2	L1 near6 (select$6 or multiplex$6)	7714	L2
L1	(arithmetic$3 or carry or overflow$3 or zero or sign) near5 (bit$1 or flag$1)	88501	L1

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   IEE CNF   IEE Conference   ☐   **1. Design of synchronous and asynchronous variable-latency pipelined multipliers**
              Proceeding   Olivieri, M.;
   IEEE STD   IEEE Standard   Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
                                                  Volume 9, Issue 2, April 2001 Page(s):365 - 376

                                                  AbstractPlus | References | Full Text: PDF(344 KB)   IEEE JNL

                                         ☐   **2. Bit-sliced median filter design based on majority gate**
                                                  Lee, C.L.; Jen, C.-W.;
                                                  Circuits, Devices and Systems, IEE Proceedings G
                                                  Volume 139, Issue 1, Feb. 1992 Page(s):63 - 71

                                                  AbstractPlus | Full Text: PDF(572 KB)   IEE JNL

                                         ☐   **3. A VLSI architecture for gray-scale morphological filtering and its application**
                                                  Charng Long Lee; Jzong-Shin Chen; Chein-Wei Jen;
                                                  Circuits and Systems, 1991., IEEE International Sympoisum on
                                                  11-14 June 1991 Page(s):2100 - 2103 vol.4

                                                  AbstractPlus | Full Text: PDF(404 KB)   IEEE CNF

                                         ☐   **4. Synchronous up/down counter with clock period independent of counter size**
                                                  Stan, M.R.;
                                                  Computer Arithmetic, 1997. Proceedings., 13th IEEE Symposium on
                                                  6-9 July 1997 Page(s):274 - 281

                                                  AbstractPlus | Full Text: PDF(608 KB)   IEEE CNF

                                         ☐   **5. A joint source-channel coding scheme for robust image transmission**
                                                  Chande, V.; Farvardin, N.;
                                                  Data Compression Conference, 1998. DCC '98. Proceedings
                                                  30 March-1 April 1998 Page(s):530

                                                  AbstractPlus | Full Text: PDF(76 KB)   IEEE CNF

                                         ☐   **6. Bit-width selection for data-path implementations**
                                                  Carreras, C.; Lopez, J.A.; Nieto-Taladriz, O.;
                                                  System Synthesis, 1999. Proceedings. 12th International Symposium on
                                                  10-12 Nov. 1999 Page(s):114 - 119

                                                  AbstractPlus | Full Text: PDF(116 KB)   IEEE CNF

7. **High-performance cellular automata random number generators for embedded probabilistic computin**
Shackleford, B.; Tanaka, M.; Carter, R.J.; Snider, G.;
Evolvable Hardware, 2002. Proceedings. NASA/DoD Conference on
15-18 July 2002 Page(s):191 - 200

AbstractPlus | Full Text: PDF(820 KB)   IEEE CNF

8. **A practical consistent-quality two-pass VBR video coding algorithm for digital storage application**
Hai Bing Yin; Xiang Zhong Fang; Li Chen; Jun Hou;
Consumer Electronics, IEEE Transactions on
Volume 50, Issue 4, Nov. 2004 Page(s):1142 - 1150

AbstractPlus | Full Text: PDF(595 KB)   IEEE JNL

9. **Fast sequential decoding algorithm based on dynamic searching strategy**
Lee, C.-Y.; Yang, W.-W.; Jeng, L.-F.;
Communications, IEE Proceedings-
Volume 141, Issue 5, Oct. 1994 Page(s):312 - 316

AbstractPlus | Full Text: PDF(376 KB)   IEE JNL

10. **Experimental evaluation of an open-loop all-optical chaotic communication system**
Argyris, A.; Kanakidis, D.; Bogris, A.; Syvridis, D.;
Selected Topics in Quantum Electronics, IEEE Journal of
Volume 10, Issue 5, Sept.-Oct. 2004 Page(s):927 - 935

AbstractPlus | References | Full Text: PDF(624 KB)   IEEE JNL

11. **Search of optimum gas mixture ratio as gas insulating medium by genetic algorithm**
Cho, M.; Ishiyama, S.; Ohtsuka, S.; Hikita, M.;
Dielectrics and Electrical Insulation, IEEE Transactions on [see also Electrical Insulation, IEEE Transactions (
Volume 11, Issue 2, Apr 2004 Page(s):334 - 347

AbstractPlus | Full Text: PDF(1259 KB)   IEEE JNL

12. **Wavelet packet filterbanks for low time delay audio coding**
Philippe, P.; de Saint-Martin, F.M.; Lever, M.;
Speech and Audio Processing, IEEE Transactions on
Volume 7, Issue 3, May 1999 Page(s):310 - 322

AbstractPlus | References | Full Text: PDF(236 KB)   IEEE JNL

13. **Performance of closed-loop power control in DS-CDMA cellular systems**
Chockalingam, A.; Dietrich, P.; Milstein, L.B.; Rao, R.R.;
Vehicular Technology, IEEE Transactions on
Volume 47, Issue 3, Aug. 1998 Page(s):774 - 789

AbstractPlus | References | Full Text: PDF(568 KB)   IEEE JNL

14. **Determining parameters to minimize jitter generation in the SRTS method**
Walker, J.; Cantoni, A.;
Communications, IEEE Transactions on
Volume 46, Issue 1, Jan. 1998 Page(s):82 - 90

AbstractPlus | References | Full Text: PDF(240 KB)   IEEE JNL

15. **A versatile function generator chip implemented in an I/SUP 2/L gate array**
Bahraman, A.; Levie, J.H.; Chang, S.Y.S.; Hopkins, M.A.; Hartmann, R.A.; Srour, J.R.;
Solid-State Circuits, IEEE Journal of
Volume 17, Issue 4, Aug 1982 Page(s):671 - 676

AbstractPlus | Full Text: PDF(1104 KB)   IEEE JNL

16. **An integration of all refractory Josephson logic LSI circuit**
Kosaka, S.; Shoji, A.; Aoyagi, M.; Shinoki, F.; Tahara, S.; Ohigashi, H.; Nakagawa, H.; Takada, S.; Hayakawa
Magnetics, IEEE Transactions on

Volume 21, Issue 2, Mar 1985 Page(s):102 - 109

AbstractPlus | Full Text: PDF(1216 KB)   IEEE JNL

17. **Combined M-ary code shift keying/binary pulse position modulation for ultra wideband communicatio**
Erkucuk, S.; Dong In Kim;
Global Telecommunications Conference, 2004. GLOBECOM '04. IEEE
Volume 2, 29 Nov.-3 Dec. 2004 Page(s):804 - 808 Vol.2

AbstractPlus | Full Text: PDF(522 KB)   IEEE CNF

18. **Reliable transmission of MPEG-2 VBR video streams over new network adaptation and ATM adaptatio**
Garcia, X.; Olivier, A.; Verscheure, O.; Frossard, P.;
IEEE ATM Workshop 1997. Proceedings
25-28 May 1997 Page(s):158 - 167

AbstractPlus | Full Text: PDF(716 KB)   IEEE CNF

19. **Parity sensitive comparators**
Fabregat, G.; Marti, J.V.; Leon, G.;
Dependable Computing, 1999. Proceedings. 1999 Pacific Rim International Symposium on
16-17 Dec. 1999 Page(s):53 - 59

AbstractPlus | Full Text: PDF(100 KB)   IEEE CNF

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